MIMO Switched-capacitor DC-DC Converters using only Parasitic Capacitances through Scalable Parasitic Charge Redistribution

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***Abstract*—This work presents a multiple-input multiple-output (MIMO) switched-capacitor (SC) DC-DC converter that only uses the parasitic capacitance already present in fully integrated SC power converters to generate multiple DC voltages. When used in an SC converter together with the scalable parasitic charge redistribution (SPCR) technique, the presented MIMO converter provides additional voltage rails which can be used to power gate drivers or control blocks without any area overhead. Moreover, because the proposed converter only makes use of elements which are already present in fully integrated SC converters, only conductive losses are introduced. This means that, for low output powers, efficiencies arbitrarily close to 100% can be achieved. The presented type of converter is characterized using a MIMO model which is in turn used to prove the efficiency of the converter compared to regular SC MIMO converters, particularly for a large number of inputs or outputs. Measurements verify the basic working principle of the presented converter, demonstrating a peak efficiency of 98.9% and output powers sufficient to power internal converter blocks.**

***Index Terms*—Switched-Capacitor, DC-DC, Power Converter, Power Management, Parasitic, Bottom-Plate capacitance, MIMO, Fully Integrated, High efficiency, Low-power**

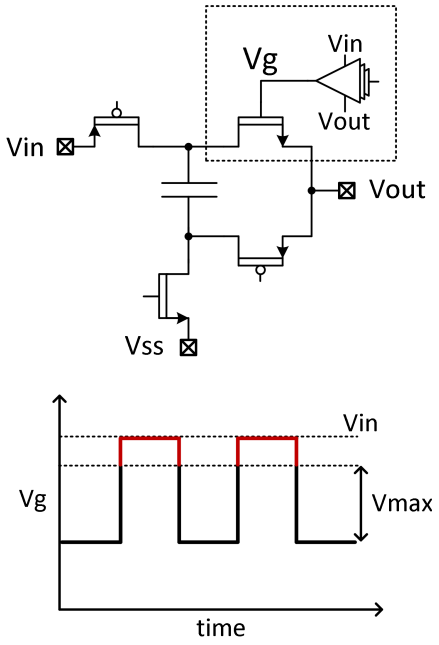

Fig. 1. Example gate driving scheme for a topside transistor in a 2:1 SC DC-DC converter. With large Vin, the transistor's voltage rating is no longer respected.

I. Introduction

In recent years there has been an increasing interest in fully- or partly-integrated DC-DC conversion. Bringing the power management unit (PMU) closer to the application reduces the system size, shortens the bill-of-materials (BoM) and can significantly improve the overall system efficiency [1]–[7]. Switched-capacitor (SC) converters in particular are well-suited for high levels of integration due to the simple fact that both transistors and capacitors are readily available in modern technology nodes. Moreover, because both are essential in digital systems, their quality increases naturally with reduced node size, leading to improved performance with technology scaling [8]. Thanks to these advantages, SC converters have become popular in literature [9] and now span a wide range of specifications, from very high power density [10]–[12] or efficiency [13]–[15] to large voltage conversion ratio's (VCR's) [16], [17], and have been used for many different applications, including mobile [18], [19], MEMS [20] and the internet-of-things (IoT) [21]–[23]. In spite their popularity, however, there are still many research directions to be explored and issues to be solved, two of which are touched upon in this paper.

While switches are often idealized in early stages of the design of an SC converter, at one point they need to be translated to transistors that require appropriate gate-driving signals. For converters with a low in- and output voltage relative to the technology's supply voltage, this can be accomplished by directly using a combination of the ground, in- and/or output voltage. With larger in- and/or output voltages, however, said combination might no longer suffice to drive the transistor's gate

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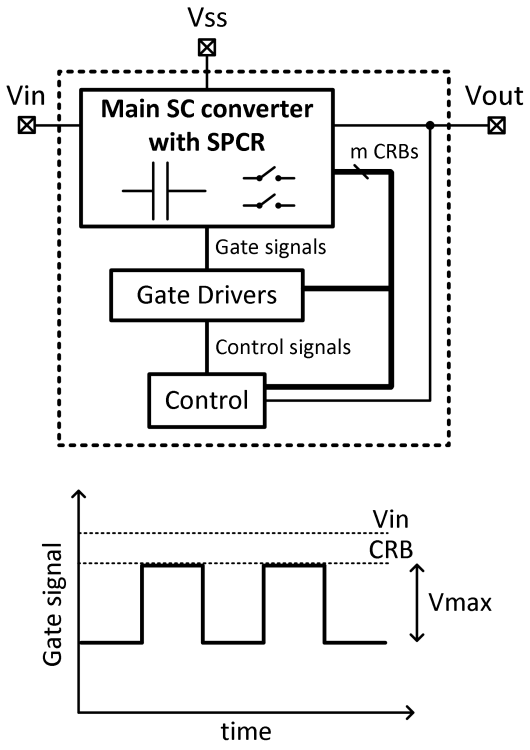

Fig. 2. High level schema of an example system that uses m CRB's, generated by the SPCR technique, to power gate drivers and the converter controller.

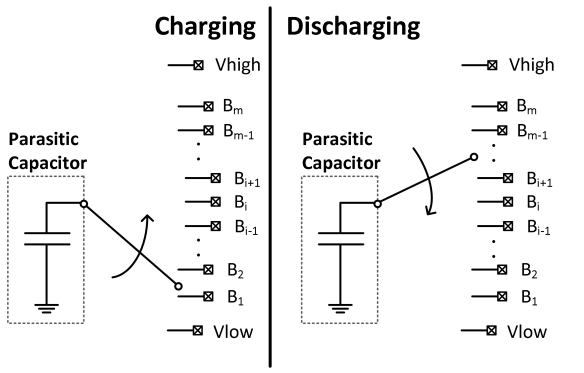

Fig. 3. Working principle of SPCR technique from the point of view of a single parasitic capacitor.

while also respecting its maximum voltage rating, as illustrated by Fig. 1. In these situations, additional voltage rails are thus a necessity, but even when they are not, they can be advantageous if they increase the power transistors' overdrive voltage. In literature, these voltage rails are typically generated using either a separate DC-DC converter per rail [18], or one larger multiple-input-multiple-output (MIMO) DC-DC converter [12]. For other applications, such multiple-output converters have also been successfully adopted [24]–[26], showing the promise of this technology. Alternatively, a bootstrap circuit can be used to create a voltage relative to the transistor's source node [16]. Either way, the generation of extra rails takes up a substantial part of the die area, may even require additional external components [24], [25], increases the total system complexity, and generally only achieves limited efficiency.

A second open research question are the overhead losses of ultra-low-power converters. Here, the output power is generally so low that the overhead (control, clock generation, etc.) has proven to be a bottleneck for the achievable efficiency [6]. This is especially problematic considering these kinds of converters are most-often used for severely energy-limited applications like energy scavenging or harvesting [27], where efficiency is the most important specification. In these situations, lowering the supply voltage of most of the overhead circuitry by using an additional voltage rail could lead to a significant reduction of both dynamic- and static power losses. Furthermore, due to the low control frequencies of low-power converters, large reductions of the supply voltage are possible before running into problems with the overhead's timing requirements. As before, however, the generation of the rail itself is a burden.

In [14] a technique called Scalable Parasitic Charge Redistribution (SPCR) is introduced that significantly increases the efficiency of SC converters by redistributing charge between parasitic capacitors. Exploring the SPCR technique, a series of DC voltage levels that are evenly spread across the flying capacitors' Bottom-Plate (BP) swing can easily be implemented. This paper proposes using these intrinsically-generated DC voltages, also called charge redistribution buses (CRBs), to efficiently power circuits within the converter, such as the ones described above, without any area overhead or added complexity. Figure. 2 illustrates how such an implementation could look like.

This paper is organized as follows: Section II deals with the parasitic MIMO converter's basic working principle. This type of converter's characterization and regulation is discussed in Section III, and compared to regular SC MIMO converters in Section IV. Section V discusses measurement results of the presented converter and Section VI summarizes this work.

II. Working Principle

In Fig. 3 the working principle of SPCR from the point-of-view of the parasitic capacitor is shown. Rather than continuously switching between V_{high} and V_{low}, the capacitor will instead connect to intermediate voltage rails B_1 to B_m in ascending order when charging and descending order when discharging. In order to explain how this results in a series of DC voltage rails, it

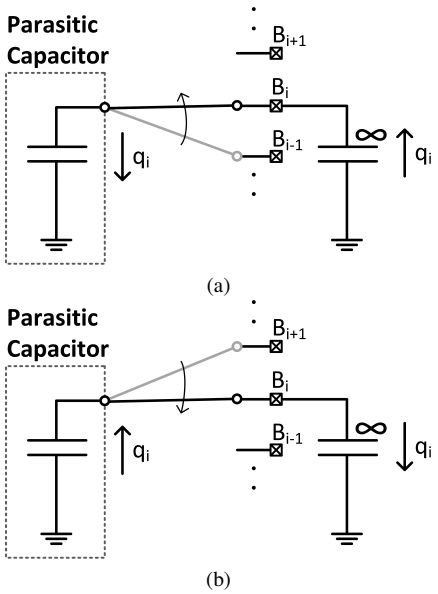

Fig. 4. Working principle of SPCR technique from the point of view of a single intermediate voltage rail, B_i, during (a) the charging- and (b) the discharging phase of the parasitic capacitor.

helps to assume an infinite decoupling capacitor at each rail as shown in Fig. 4. When the parasitic capacitor, C_{par}, connects to B_i in its charging phase, an amount of charge, dependent on the difference between the rail's voltage, V_i, and the previous rail's voltage, V_{i-1}, is transferred. Similarly, in the discharging phase, the transferred charge depends on $(V_{i+1} - V_i)$. Assuming B_i is unloaded, the sum of the charges of both phases must be zero when the system is in steady-state. This means that the following must be true:

$$V_i = \frac{V_{i+1} + V_{i-1}}{2}. \tag{1}$$

In other words, if B_i is unloaded, then its voltage will converge to the average of the adjacent nodes' voltages. This property, while simple, is key to understanding this type of MIMO converter and is used throughout this paper.

Now, if all intermediate nodes are unloaded, (1) can be used to prove that said nodes will spread out evenly between the boundary conditions set by V_{high} and V_{low}:

$$V_i = \frac{i}{m+1}\Delta V + V_{low}, \tag{2}$$

where ΔV is the voltage difference between V_{high} and V_{low}. Thus, from two reference voltages V_{high} and V_{low}, the parasitic converter can generate any number of desired DC nodes using nothing but the parasitic coupling of a main SC converter. Simply by adding more intermediate steps, more DC voltages are generated.

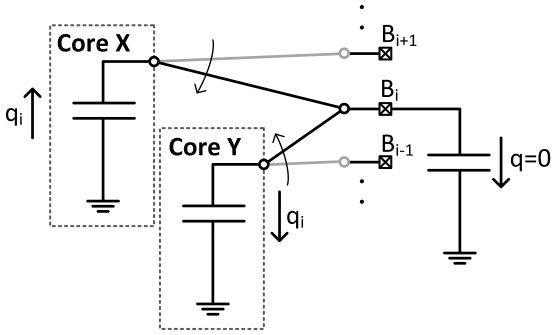

Fig. 5. Working principle of SPCR technique in steady-state using phase-shifted cores.

In practice, very large decoupling capacitors are impractical and costly to realize. However, it is possible to achieve the same effect without decoupling. After all, the purpose of the decoupling capacitor is simply that of a buffer: it holds a certain amount of charge until it is required again by the parasitic converter. As such, one can argue that the parasitic capacitor is exchanging charge with a time-shifted version of itself. By splitting the parasitic capacitor up into multiple phase-shifted versions of itself, each phase can at each point in time connect to another that goes through the opposite voltage step [14], as shown in Fig. 5, and the middleman can be cut. Thus, when using the SPCR technique, the extra voltage rails require no decoupling and are by consequence truly generated without area overhead.

III. Characterization and Regulation

Before getting into further analysis, it is important to emphasize the situation for which we are analyzing this type of SC converter. In the context of a main converter that requires certain output voltages internally, the proposed converter can be used without the addition of any circuitry, which means that, unlike with a regular SC converter, non-conductive losses (bottom-plate losses, gate charging, leakage, etc.) are not introduced. In the parasitic converter there is, on the other hand, always a transfer of charge, even when none of its output nodes are loaded. The losses associated with these charge transfers, however, are the bottom-plate losses of the main converter and are thus not considered in further analysis. After all, they are already taken into account in the design of the main converter. What is investigated instead is how adding a load on one of the intermediate nodes generated by SPCR increases the total power consumption of the main converter, $P_{mainconverter}$. The change in power is considered to be the true parasitic converter input power:

$$P_{in} = \Delta P_{mainconverter}. \tag{3}$$

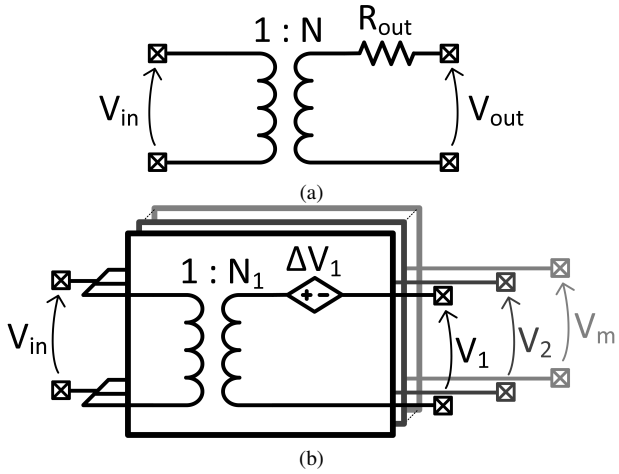

Fig. 6. Model of an SC converter with (a) a single output, and (b) multiple ports.

A. General MIMO SC Model

In Fig. 6a the typical model of a single-output SC converter is shown [28]. In this model, infinite decoupling is assumed to be present at the output, which means that the output voltage is perfect DC while the output current is time-averaged. Also, note that the converter in this general model consists of ports, with each port having a positive and a negative terminal. In practice, though, both ports will often share their negative terminal.

If no parasitic elements are present, only two parameters suffice to fully characterize a converter. The VCR, N, determines the relation between in- and output voltage, while the output resistance, R_{out}, relates the voltage drop, ΔV_{drop}, at the output, to the current that is drawn from it:

$$\Delta V_{drop} = R_{out} I. \tag{4}$$

The single-output converter's conductive losses are determined by the latter:

$$P_{loss} = R_{out} I^2. \tag{5}$$

Whereas in the above discussion the terms input and output are used, from an energy perspective the input and output are not determined by the topology but by the sign of the time-averaged current. For example, if the time-averaged current in (4) changes sign, what was considered the output will in fact be sourcing charge and thus current.

When generalizing this model to multiple ports it becomes apparent that the complexity can not scale linearly with the number of ports, m. This is due to the fact that a load current supplied to a port can influence the voltage across every other port's terminals. However, it still does so in linear fashion. Figure 6b shows the model proposed in [29]. Here, the voltage drop across the terminals of port i, ΔV_i, is shown to be

$$\Delta V_i = \sum_{j=1}^{m} z_{ij} I_j, \tag{6}$$

where I_j is the time-averaged load current supplied to port j, and z_{ij} is the transimpedance from the time-averaged current supplied to port j to the voltage across the terminals of port i. The full system can consequently be described by a simple algebraic equation

$$\vec{V} = \vec{N} V_{in} - \mathbf{Z}\vec{I}, \tag{7}$$

with V_{in} the voltage across the input port's terminals as shown in Fig. 6b, $\vec{V}$, $\vec{N}$ and $\vec{I}$ vectors containing the respective voltage, conversion ratio and time-averaged current for each port, and $\mathbf{Z}$ the converter's impedance matrix, whose elements are the transimpedances used in (6). Similar to the single-output case, the total conduction losses can be written as

$$P_{loss} = \vec{I}^T \mathbf{Z} \vec{I}. \tag{8}$$

Note that, similar to the two-port case, each port can source or sink current to the system, depending on the sign of its corresponding current. As such, this model describes MIMO operation.

B. Characterization

Within the context of a main converter using SPCR, the switches that connect the parasitic capacitor to the different intermediate nodes should be large enough to allow close to full settling of the capacitor's voltage to enable the full reduction in bottom-plate losses [13]. Therefore, the parasitic converter is assumed to operate in the slow-switching limit (SSL) [28], where the switch resistance can be neglected.

In [29] a method is described to work out $\mathbf{Z}$ given an SC converter's topology by using a charge-based analysis for each node separately. Due to the highly regular structure of the parasitic MIMO converter, however, it is possible to derive the elements of $\mathbf{Z}$ directly using a more intuitive approach.

Consider an example parasitic converter with 6 intermediate nodes. Each node is the positive terminal of a port, with the corresponding negative terminal being V_{low} for all ports. Figure 7 illustrates how the node voltages shift when a single load is introduced. For all nodes without a load, the relation described by equation (1) still holds. At the loaded node, on the other hand, a certain amount of charge flows to the load each

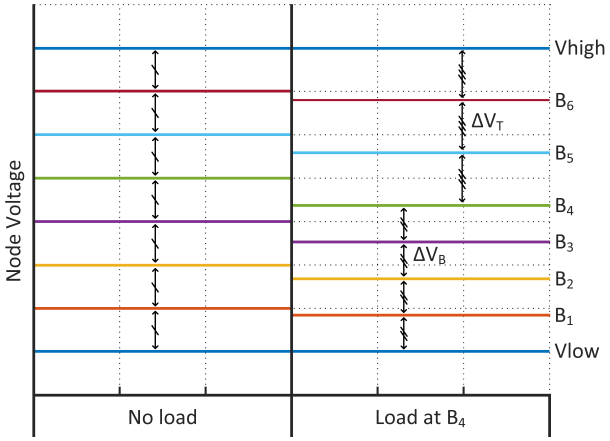

Fig. 7. Waveforms of the node voltages of a 6 node parasitic MIMO SC converter under no-load-, and loading conditions.

clock cycle, and will pull said node down. Thus, the load changes the voltage differences between the nodes. Above the loaded node, the voltage difference, ΔV_T, will be enlarged, while the opposite is true for the voltage difference of the bottom nodes, ΔV_B. Using the condition of charge preservation in steady-state at the loaded node, j, the relation between both can be written as

$$\Delta V_T = \Delta V_B + \frac{q_{L,j}}{C_{tot}}, \tag{9}$$

where $q_{L,j}$ is the load charge over an entire clock period and C_{tot} is the total capacitance of the parasitic converter. Regardless of the size of the load, the sum of all voltage differences must, of course, still be equal to the total ΔV. By using this fact together with (9), the following can be derived:

$$\Delta V_T = \frac{\Delta V}{m+1} + \frac{j}{m+1}\frac{q_{L,j}}{C_{tot}}, \tag{10}$$

$$\Delta V_B = \frac{\Delta V}{m+1} + \left(\frac{j}{m+1} - 1\right)\frac{q_{L,j}}{C_{tot}}, \tag{11}$$

which in turn can be used to determine the voltage of any node, i,

$$V_i = \begin{cases} V_{low} + \frac{i}{m+1}\Delta V + j(\frac{i}{m+1} - 1)\frac{q_{L,j}}{C_{tot}} & i > j \\ V_{low} + \frac{i}{m+1}\Delta V + i(\frac{j}{m+1} - 1)\frac{q_{L,j}}{C_{tot}} & i \leq j. \end{cases} \tag{12}$$

Considering the fact that the time-averaged load current drawn from a node equals $f_{sw}q_{L,j}$, where f_{sw} is the converter frequency corresponding to a full clock cycle, all elements of the impedance matrix $\mathbf{Z}$ can subsequently be derived:

$$z_{ij} = \begin{cases} j(1 - \frac{i}{m+1})\frac{1}{f_{sw}C_{tot}} & i > j \\ i(1 - \frac{j}{m+1})\frac{1}{f_{sw}C_{tot}} & i \leq j. \end{cases} \tag{13}$$

Table I shows the impedance matrix for a select number of output nodes.

C. Natural Regulation

The parasitic converter's frequency is set by the frequency of the main converter. At first glance, it might seem like this makes regulation of the parasitic converter's intermediate nodes difficult to achieve. In practice, though, this inherent sharing of working frequency leads to an interesting benefit of the proposed converter which the authors refer to as natural regulation.

In a SC converter, there are many overhead loss contributors whose power consumption scales largely linearly with the converter's switching frequency. Such contributors include gate driver, phase generators, interconnect buffers, etc. . When these blocks are powered by the intermediate voltage rails, they will only require energy when the main converter is switching, as pointed out in [12]. In the presented case, however, energy will be transferred to the intermediate rails whenever the main converter switches by means of the parasitic converter. As such, regulation is achieved naturally without overhead.

For overhead loss contributors that demand energy regardless of the main converter's switching frequency, e.g. a hysteretic controller's comparator, the main converter will need to realize a minimal switching frequency in order to meet the minimum voltage requirements for these blocks. This situation, though, is not very different from that of a converter whose control is powered by its own output voltage. Also here, the converter will be switching every so often to power its overhead circuitry.

IV. Topology Comparison

In this section, the presented parasitic MIMO topology is compared to two regular SC MIMO topologies based on the commonly-used Ladder- [12], [30] and Dickson topologies, shown in Fig. 8a and Fig. 8b respectively. The negative terminal of all ports is assumed to be V_{low}. By consequence, the discussion can be simplified to one of the positive terminals or nodes.

A. Losses

A switched capacitor converter's losses can be divided into two groups: Conductive losses due to its finite output resistance and non-conductive losses such as power transistor leakage, gate-charging losses and parasitic substrate coupling losses. Because the parasitic

TABLE I
PARASITIC CONVERTER'S NORMALIZED IMPEDANCE MATRIX FOR VARYING NUMBER OF OUTPUT NODES

m	1	2	3	4	5
$f_{sw}C_{tot}\mathbf{Z}$	$\frac{1}{2}$	$\frac{1}{3}\begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix}$	$\frac{1}{4}\begin{bmatrix} 3 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 3 \end{bmatrix}$	$\frac{1}{5}\begin{bmatrix} 4 & 3 & 2 & 1 \\ 3 & 6 & 4 & 2 \\ 2 & 4 & 6 & 3 \\ 1 & 2 & 3 & 4 \end{bmatrix}$	$\frac{1}{6}\begin{bmatrix} 5 & 4 & 3 & 2 & 1 \\ 4 & 8 & 6 & 4 & 2 \\ 3 & 6 & 9 & 6 & 3 \\ 2 & 4 & 6 & 8 & 4 \\ 1 & 2 & 3 & 4 & 5 \end{bmatrix}$

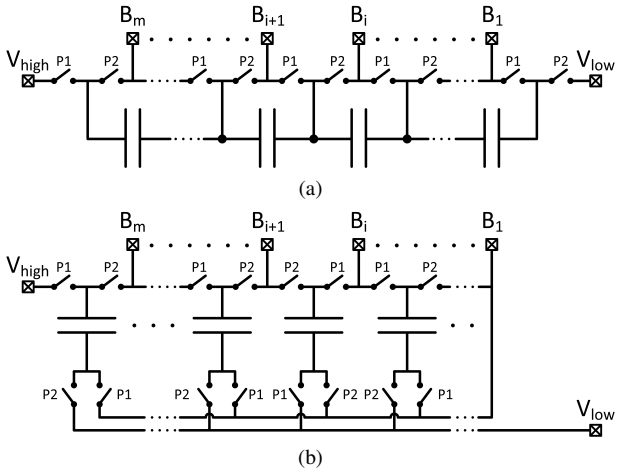

Fig. 8. Generalized topology of the (a) Ladder- and (b) Dickson MIMO converters.

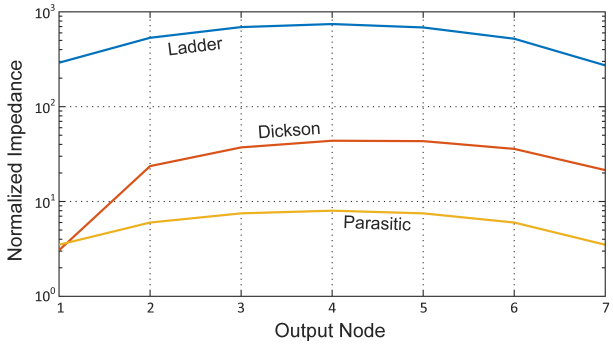

Fig. 9. Comparison of the sum of normalized output impedances per output node for different SC MIMO converters with 7 nodes.

TABLE II
OVERVIEW OF CURRENT PROFILES

Use Case	$\vec{I}$
Iso-current	$\frac{2}{m}\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}^T$
Iso-power	$\frac{m+1}{m}\begin{bmatrix} 1 & \frac{1}{2} & \cdots & \frac{1}{m} \end{bmatrix}^T$
Single-output VCR=0.5	$\begin{bmatrix} 0 & \cdots & 0 & 2 & 0 & \cdots & 0 \end{bmatrix}^T$

converter does not add any power transistors, nor flying capacitance to the system, it will neither add leakage-, gate-charging- and parasitic substrate coupling losses. As such it has a significant head-start compared to regular SC topologies.

The output resistance of a SC converter has an SSL and fast-switching limit (FSL) component [28], often referred to as SSL- and FSL-resistance. As established in Section III-B, due to the sizing of the switches of the parasitic converter, it is assumed to work in the SSL regime, where the FSL-component can be neglected. As such, the comparison here focuses on the SSL-resistance.

For a single-output converter, different topologies can be evaluated by simply comparing their SSL topology factors, K_c, to one another [13], [31]. These are in essence their SSL-resistance [28], but normalized for switch frequency and total flying capacitance [13]. After all, a topology with a larger output resistance will have larger conductive losses for the same load current. As such, single-output converters can be ordered in terms of SSL performance, regardless of the nature of the load.

For MIMO converters, on the other hand, evaluation is not as clear-cut. As demonstrated by (8), the conductive losses depend on $\vec{I}$, which means that, even after normalization, the relative sizes of the currents drawn from the nodes have a significant impact on a direct comparison. As a result, while the size of the elements of the impedance matrix, $\mathbf{Z}$, can give an initial impression, any general comparison of topologies must also include multiple specific use cases for the converter.

1) Element based: Figure 9 gives a first element-based comparison of the different topologies for 7 output nodes. Similar to the single-output case, the impedance elements are normalized by multiplying them with the switching frequency and total capacitance. The Dickson topology has the lowest normalized impedance of all converters in output 1, which is the node with the lowest voltage. This result matches earlier single-output analysis [28]. For every other node, however, the parasitic converter has significantly lower output impedance: four to six times better compared to the Dickson-, and two orders of magnitude better compared to the Ladder converter.

2) Use Case based: The topologies' normalized conductive losses are compared for three different node current profiles, each of which corresponds to a specific use case. Table II gives an overview of the used current profiles, which are, unlike in [32], further normalized such that the total output power in each case is the same. These consist of two multiple-output cases and one where the MIMO converter is used to supply a single voltage corresponding to a VCR of 2:1. The results of this comparison are shown in Fig. 10. When used with 2 or fewer outputs, the parasitic converter shows higher losses than the Dickson converter. For a larger number of outputs, on the other hand, the regular converters see a rapid increase in losses. The relative gain of the proposed converter gets consequently larger for increasing number of outputs. Moreover, this statement holds regardless of the use-case for which the topologies are compared. Thus it can be concluded that the parasitic converter has exceptionally low losses.

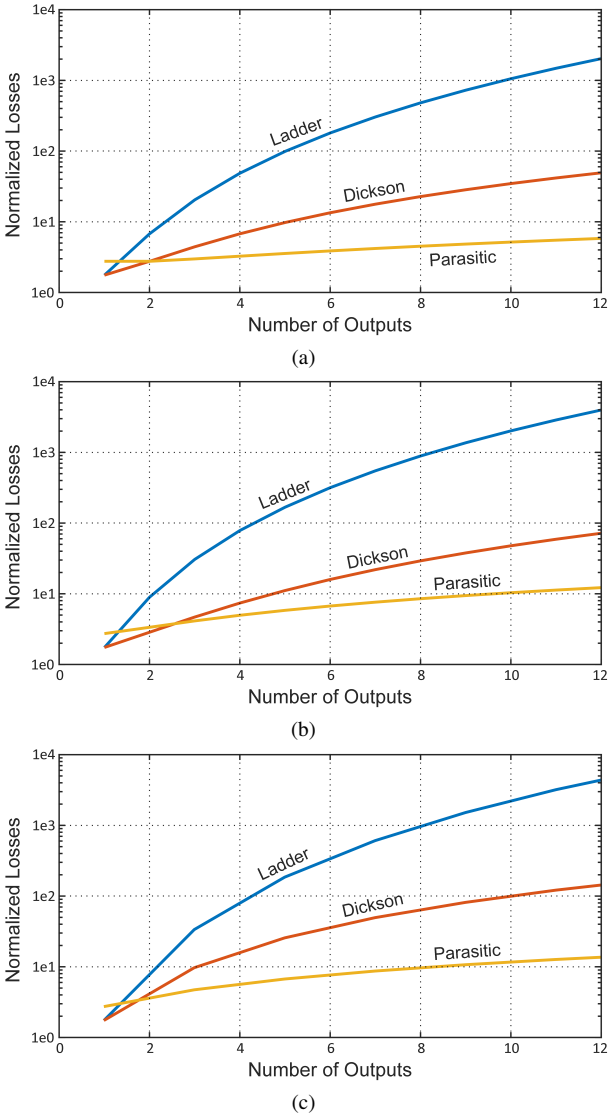

Fig. 10. Comparison of the normalized conduction losses of the parasitic-, to the ladder- and Dickson MIMO SC converter for (a) an equal load current drawn from each node, (b) a load current drawn from each node inversely proportional to the VCR and (c) a single load current drawn from a VCR of 2:1.

B. Transient Behavior

The transient behavior of the proposed-, ladder- and Dickson topologies are compared for an implementation with nine intermediate nodes. In order to be able to remove the load capacitance of every intermediate node, the ladder- and Dickson converter are implemented as two converter cores which run in antiphase. This way there is always at least one capacitor connected to every node. In addition, the switch resistance is assumed to be close to zero such that all converters run fully in the SSL region.

Figure 11 shows the simulated transient response of the intermediate nodes corresponding to a VCR of 10:9 and 2:1, when a load step is applied to the intermediate node with a VCR of 10:9. Both in cross- (Fig. 11a) and self-regulation (Fig. 11b) situations the parasitic converter undergoes the smallest voltage deviation at 2mV and 2.9mV respectively due to its low output impedance. The Dickson- with a respective deviation of 15mV and 23mV, and the ladder-converter, with a 207mV and 87mV drop respectively, do notably worse.

In addition, the parasitic converter has significantly lower ripple. Under self-regulation, for example, its ripple is only 2.2mV, compared to 18.7mV and 23.9mV for the Dickson- and ladder converter respectively. When a load is applied to a node, the other intermediate nodes of the parasitic converter show no ripple. This is due to the fact that at no point in time a capacitor of the parasitic converter connects to more than one node at the same time. As such, no low-impedant current path exists between any pair of nodes, leading to a high degree of isolation.

Figure 12 compares the line regulation of the same intermediate nodes, under a line droop of 21mV that settles within 120ns, which is representative of the droop of the main converter in [14]. At the intermediate node corresponding to a VCR of 10:9, the Dickson converter has the smallest droop of 1.6mV. The ladder- and parasitic converter, on the other hand, have droops of 13.9mV and 5.7mV respectively. It is worth noticing that the parasitic converter has a delayed response to the line droop. This is due to the earlier discussed isolation between the intermediate nodes, which also extends to the V_{high} node: It is only when the core, which was connected to V_{high}, switches to the aforementioned intermediate node, that said node's voltage deviates. Furthermore, in doing so it connects to a core that has not yet connected

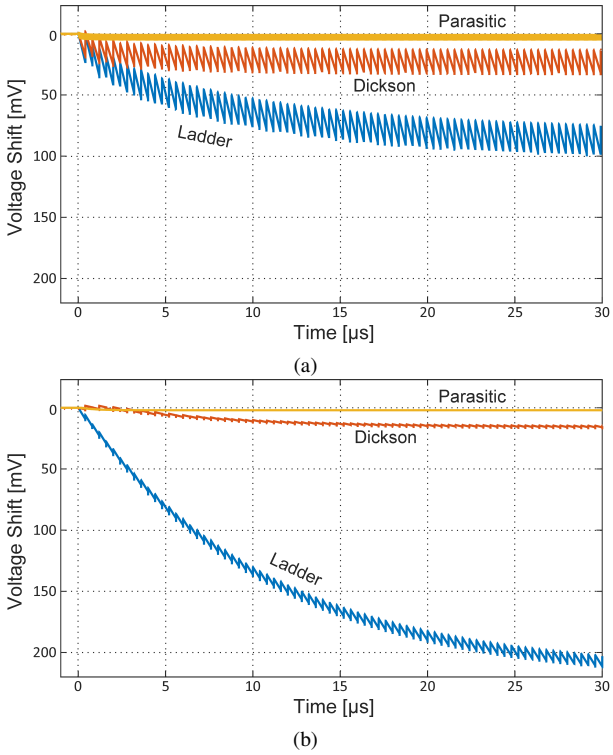

Fig. 11. Comparison of the simulated voltage shift waveforms of the intermediate nodes corresponding to a VCR of (a) 10:9 and (b) 2:1, for a parasitic-, ladder- and Dickson-converter with a total of 9 intermediate nodes, when a load step of $500nA$ is applied to the intermediate node with a VCR of 10:9 at $t = 0s$. Here, the total flying capacitance is $100pF$ and $f_{sw} = 1.25MHz$.

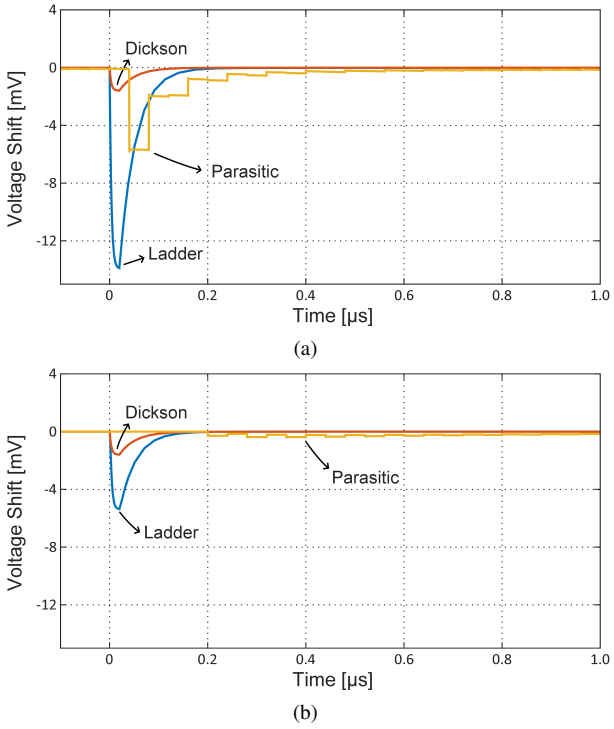

Fig. 12. Comparison of the simulated voltage shift waveforms of the intermediate nodes corresponding to a VCR of (a) 10:9 and (b) 2:1, for a parasitic-, ladder- and Dickson-converter with a total of 9 intermediate nodes, when a droop is applied to the input at $t = 0s$, representative of the droop reported in [14]. Here, the total flying capacitance is $100pF$ and $f_{sw} = 1.25MHz$.

to a perturbed node, leading to the voltage deviation being averaged out. This also means by extension that intermediate nodes with a smaller VCR (10:8, 10:7, ...) have increasingly better isolation from line transients because a core goes through more averaging steps before connecting with said nodes. This is demonstrated by Fig. 11b. As can be seen, the node corresponding to a VCR of 2:1 has a significantly delayed response and a voltage perturbation less than 0.4mV.

V. Measurements

To verify the working principle and quantitative analysis of the parasitic converter, measurements were performed on a fully integrated 2:1 converter which had its main converter results published in [14]. In this work the focus is the use of the intrinsically generated DC voltages as usable voltage rails that can support power delivery.

A schematic representation of the parasitic converter within the main converter is given in Fig. 13. The converter uses a total of 16 out-of-phase cores to generate 9 output nodes between 900mV and ground. The B_5 node, corresponding to a VCR of 2:1, however, was not implemented as a physical voltage rail in this

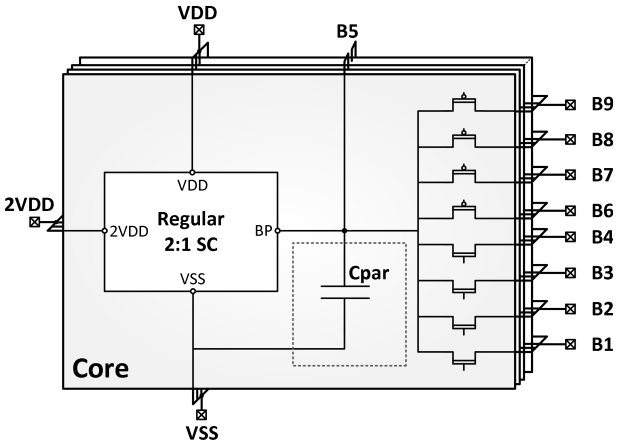

Fig. 13. System overview of the MIMO SC converter using only parasitic capacitances within a main converter.

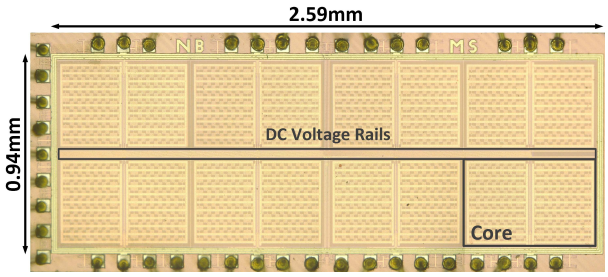

Fig. 14. Die micrograph of fully integrated SC 2:1 converter using SPCR, measuring $2.4mm^2$ without bondpads. The intrinsically generated voltage rails are highlighted.

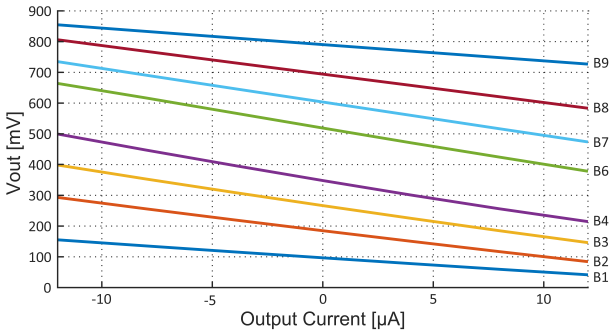

Fig. 15. Measured output voltage versus output current for all DC voltage rails with $f_{sw} = 1.6MHz$ and $V_{DD} = 900mV$.

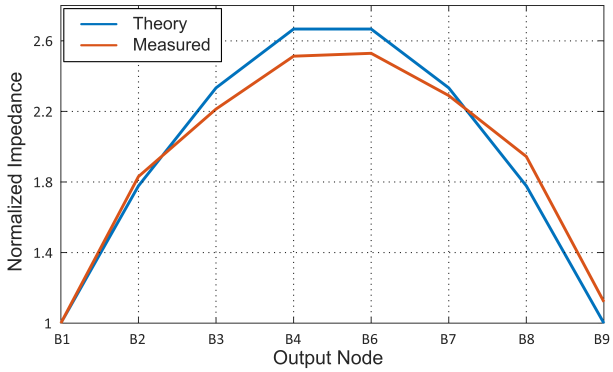

Fig. 16. Comparison of relative size of the measured output impedance of all DC nodes to theoretical predictions.

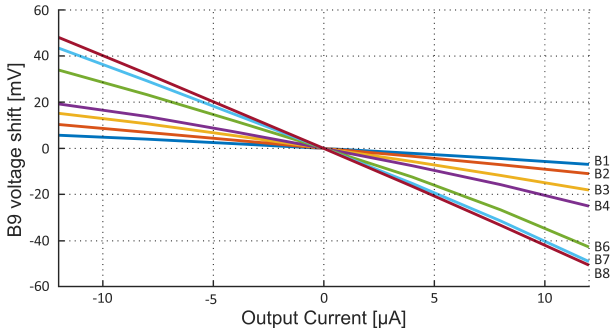

Fig. 17. Measured voltage shift on B_9 under the influence of a load current drawn from B_1 to B_8.

realization. None of the nodes has any decoupling added to it. Therefore, within this larger design, the nodes can be used without adding any area overhead. A die photograph of the realization used in the measurements is shown in Fig. 14.

All measurements unless otherwise stated are performed by connecting a 900mV voltage source to V_{DD}, which corresponds to the main converter's output. Its input, on the other hand, is left unconnected and its lower-bound hysteretic controller is bypassed by applying a reference voltage, V_{ref}, of approximately 1V. This way, the main converter is unloaded and free-running, causing its influence on measurements to be reduced as much as possible.

A. Output Impedance

Figure 15 shows the measured voltage of the DC voltage rails versus the rail current, in both source and sink conditions. The dropout voltage of the parasitic converter's nodes scale linearly with load current, as demonstrated in Section III-A. The largest and smallest absolute voltage drop at the largest measured load current of $12\mu A$ are $141mV$ and $55mV$ for B_6 and B_9 respectively, which is consistent with the findings of Section III-B. The parasitic converter's output impedance is calculated using the measured voltage deviation under loading and compared to the theoretical expected value based on the analysis of Section III-B in Fig. 16. A good match can be witnessed between both, with a maximum relative error of 10% on B_9.

To demonstrate the MIMO nature of the presented parasitic converter, the influence on the voltage of one node due to a load current on a different node is measured. These results are shown in Fig. 17 using B_9. As expected, the nodes closest to B_9 have the most impact on its voltage, causing a shift of up to $50mV$ at $12\mu A$.

B. Transient Measurement

In Fig. 18 the measured cross-regulation of the parasitic converter is shown. Here, a $50mV$ voltage step is applied to B_9 with a transient time of $50ns$. The intermediate nodes, B_8 and B_6 have a voltage shift of $18mV$ and $8mV$ respectively as a result, and settle within approximately $1\mu s$. No notable effect on B_2 is measured. As expected, the intermediate nodes closest to the perturbed node have the largest response.

Figure 19 demonstrates the line regulation of the proposed converter. Unlike for all other measurements, the input of the main converter is connected to a supply

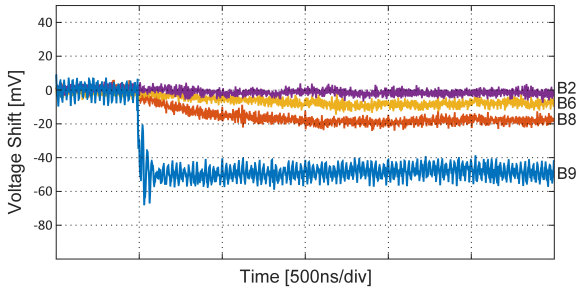

Fig. 18. Measured voltage waveforms of intermediate nodes B_2, B_6, B_8 and B_9, when a voltage step of $50mV$ is applied to B_9 with a transient time of $50ns$.

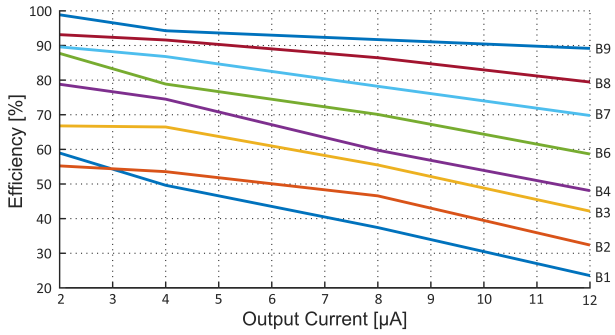

Fig. 20. Measured efficiency versus output current for B_1 to B_9 with $f_{sw} = 1.6MHz$ and $V_{DD} = 900mV$

voltage of 1.9V and the output is left unconnected. The main converter is thus active. In order to get a measurable response from the intermediate nodes, the main converter is working in open-loop configuration. The shown waveforms are the result of a $5mA$ load-step applied to the main converter with a transient time of $15ns$. Nodes B_1 to B_9 having increasingly large voltage deviations that range from $1.6mV$ to $14.4\ mV$. The settle time for all nodes was found to be approximately $1\mu s$.

C. Efficiency

In order to measure the efficiency of the parasitic MIMO converter, first a reference measurement is performed to determine the converter's current at V_{DD} under no-loading operation. By then measuring the supply current when a load current is present on one of the DC rails, and comparing said current to the reference measurement, the input power of the parasitic converter can be calculated using (3).

$$\eta_{node} = \frac{P_{node}}{\Delta P_{mainconverter}} \tag{14}$$

Figure 20 shows the resulting measured efficiency of the presented converter. Due to the conductive nature of the losses, the efficiency is largely dependent on the relative size of the load impedance to the equivalent output impedance of the converter, which means that at constant output current, a lower voltage leads to lower efficiencies. Moreover, as load current tend towards zero. the efficiency approaches 100%. The measured peak efficiency is 98.9% at a load current of $2\mu A$ at B_9. Lower load currents would have yielded even higher efficiencies, but due to the fact that the input power is calculated by subtracting two larger numbers, these measurements could not be performed with the required accuracy. The highest output power of 8.7 μW is also measured at B_9 with an efficiency of 89%. According to simulations, this power is similar to the power consumption of the main converter's controller, which is further testament to the possible use of these voltage rails within the larger converter itself.

D. Comparison

Finally, the realized parasitic converter is compared to the state-of-the-art of multiple output SC converters in Table III, for the use case described in this paper. Due to the fact that the proposed converter makes use of the parasitic substrate coupling already present in a main SC converter, it is the only one to introduce no additional die area. Moreover, this means that the converter is the only one to only have conductive losses, leading to the highest effective efficiency of 98.9%. The proposed work also achieves a high number of outputs. Unlike the compared converters, though, the parasitic converter does require a larger SC system that uses SPCR, which inherently limits its scope to the auxiliary converter use case discussed in this work.

VI. Conclusion

In this work the challenges with switched-capacitor (SC) converter's overhead losses and gate driving were discussed together with the problems associated with internal voltage rail generation. A type of multiple-input multiple-output SC converter was introduced that generates multiple DC voltages using only the parasitic capacitance already present in fully integrated SC converters. When used in a SC converter together with scalable parasitic charge redistribution (SPCR), these DC voltages can be used to provide to power low-power control blocks or gate drivers. Furthermore, because this is achieved without adding any area overhead, no additional parasitic losses (bottom-plate losses, gate-charging losses,...) are introduced. In addition, the conductive nature of the remaining losses means that efficiencies close to 100 % can be achieved for low output powers. A model for this type of MIMO converter was proposed and characterized, which was then used to compare the converter to known regular SC MIMO converters for different use cases. Especially for larger number of input- or output nodes, the presented converter was shown to

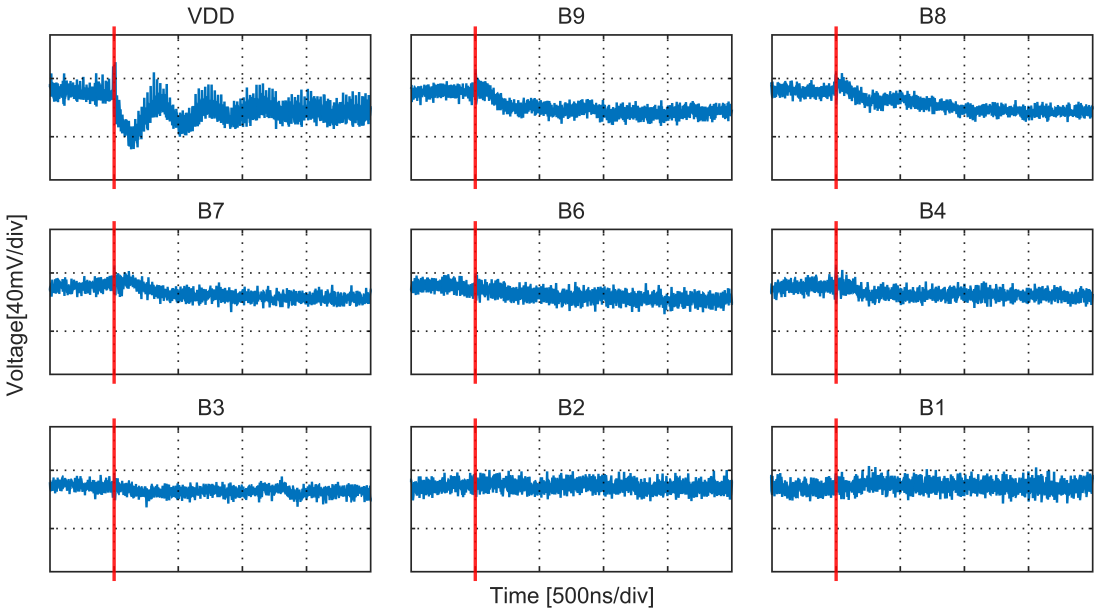

Fig. 19. Measured voltage waveforms of V_{DD} and all intermediate nodes when a $5mA$ load-step is applied to the main converter with a transient time of $15ns$.

TABLE III
COMPARISON TO STATE-OF-THE-ART.

Item	**This work**	[26]	[24]	[25]
Technology	**40nm**	90nm	350nm	65nm
Capacitors	**Parasitic Coupling**	MOS+MIM	External	MOS+External
Application	**Internal SC blocks**	Low Power SoC	Energy Harvesting	Portable Devices
V_{in} $[V]$	**0.9**	1.2	1.1-1.8	0.85-3.6
Outputs	**8**	2	2	2
V_{out}'s $[V]$	**0.09, 0.18, 0.27, 0.36, 0.54, 0.63, 0.72, 0.81**	0.32, 0.755	2, 3	0.1-1.9
η_{peak}	**98.9%***	68.6%	90%	95.8%
System η	**94.6%**	68.6%	90%	95.8%
Max P_{out}	**8.7μW**	$1mW$	$60mW$	$19mW$
Added die area	**0mm^2***	$1.65mm^2$	$6.9mm^2$	$9mm^2$
Closed-loop?	**no**	yes	yes	yes
Requirements	**Main SC converter with SPCR**	/	/	/

*effective

have particularly low losses and excellent cross- and line-regulation. The basic working principle of the presented converter was demonstrated using measurements, showing a peak efficiency of 98.9% and output powers sufficient to power internal converter blocks.

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